



S/N 08/984,562

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Jeffrey S. Mailloux et al.

Examiner: Hong C. Kim

Serial No.: 08/984,562 ✓

Group Art Unit: 2186

Filed: December 3, 1997

Docket: 303.623US3

Title: MEMORY DEVICE FOR BURST OR PIPELINED OPERATION WITH MODE
SELECTION CIRCUITRY

SUPPLEMENTAL REPLY BRIEF UNDER 37 CFR 1.193(b)

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This Supplemental Reply Brief is filed in triplicate and presented in response to the Supplemental Examiner's Answer (the "Answer") dated February 23, 2004. The Appellants respectfully request acknowledgment of receipt, and entry of this Supplemental Reply Brief in the above-identified Application for review by the United States Patent and Trademark Office Board of Patent Appeals and Interferences (the "Board").

REPLY

Related Appeals and Interferences

The Answer asserts that "... the related appeal 08/984,561 mentioned in the brief was never before the board". In the interest of accuracy, it is respectfully noted that the decision of the Examiner in this matter was appealed via presentation of an appeal brief filed on September 12, 2002. Receipt of the brief was acknowledged by the OIPE by way of a returned postcard stamped with the date September 16, 2002. After the Appellants responded to a notice of non-compliance with respect to 37 C.F.R. 1.192(c), a Notice of Allowance was received by the Appellants on March 25, 2003.

Grouping of Claims

The Answer asserts that "Applicant has not provided independent argument for each of the claims that allegedly stand alone" and "grouping of claims into ten groups is appropriate." The Appellants respectfully disagree.

In the Appeal Brief filed by the Appellants on February 10, 2003, a specific section (section c.3 found on pgs. 14-18) is devoted to discussion of the separate patentability of each

claim. At least one unique feature of each claim is presented, and it is noted for each claim that these features are not disclosed by the cited art. These reasons are bolstered by the detailed argument discussing each of the claims and their relation to the cited art on pages 7-14 of the Appeal Brief.

This type of argument is specifically approved by the M.P.E.P. § 1206, where it is stated that “The appellant must (A) state that the claims do not stand or fall together and (B) present arguments why the claims subject to the same rejection are separately patentable.” Further “The reasons may be included in the appropriate portion of the ‘Argument’ section of the brief.” See M.P.E.P. § 1206.

The standard set forth in the M.P.E.P. § 1206 has been met by the Appellants in that the following are provided: (a) a specific statement that the claims do not stand or fall together (see Appeal Brief, pg. 4, part 7), and (b) arguments as to the separate patentability of each claim, both in the form of specific statements (see Appeal Brief, pgs. 14-18, part 8, section c.3), and as a series of arguments (see Appeal Brief, pgs. 7-14, sections c.1 and c.2). Thus, the Appellants respectfully traverse the assertion in the Answer that “grouping of claims into ten groups is appropriate” and respectfully request consideration of each and every claim independently by the Board.

Compliance with 37 C.F.R. § 1.111(b)

The Answer states that the “Applicant’s arguments fail to comply with C.F.R. § 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.” The Appellants respectfully disagree.

In sections c.1.1 and c.2 of the Appeal Brief (pgs. 7 and 10), the Appellants set forth specific language which distinguishes the claims from Manning (864) and Manning (503), to wit: (a) Mannning (864) does not disclose “control logic for providing a ... mode control signal” and “a multiplexer ... for receiving ... the ... mode control signal ... therefrom and for switching the memory circuit between a burst mode and a pipelined mode” (explicitly claimed by the Appellants in claims 22-32, and 59);

(b) Manning (864) does not disclose “control logic for providing [a] ... mode control signal” that is ultimately used to switch between, or indicate, burst and pipelined modes of operation (explicitly claimed by the Appellants in claims 66-72);

(c) Manning (864) does not disclose control logic for providing an internal mode control signal (explicitly claimed by the Appellants in claim 61);

(d) Manning (503) does not disclose selecting or switching between burst and pipelined modes (explicitly claimed by the Appellants in independent claims 22, 59, 63, and 66, and in all claims that depend from them); and

(e) Manning (503) does not disclose “a multiplexer coupled to ... the control logic for receiving the ... internal mode control signal ... for switching the memory circuit between a first mode of operation and a second mode of operation” (explicitly claimed by the Appellants in claim 63).

To avoid repetitious duplication, it will simply be noted here that Manning (864) fails to disclose many other specific elements with respect to several individual claims, which are delineated on pgs. 7-8 of the Appeal Brief. An explanation as to precisely why such failure attends to the use of Manning is also included on pg. 9 of the Appeal Brief, section c.1.2 (i.e., “Why the reference does not disclose the claimed subject matter in as complete detail as is contained in the claim.”). Therefore, the Appellants respectfully traverse the assertion in the Answer that the “Applicant’s arguments fail to comply with C.F.R. § 1.111(b)” and request withdrawal of this statement.

Response by Appellants to General Arguments in the Answer

The statement in the Answer that “Manning (864) discloses a pipelined mode ... for the purpose of increasing the throughput by accessing data per every cycle” does not distinguish between the operation of a pipeline architecture (which may include a pipeline stage) and a pipeline mode, as described in detail by the Appellants (see Appeal Brief, pgs. 11-12). Similarly, the assertion in the Answer that “it would have been obvious ... to modify a standard EDO page mode of 503 with a pipelined mode of 864 because it would increase the throughput by accessing data per every cycle” does not take into account the following points made by the Appellants:

(a) neither Manning (864) nor Manning (503) disclose selecting or switching between pipelined and burst modes;

(b) the Office has admitted that "Manning [864] does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." in an Office Action mailed to the Appellants on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter; and

(c) Manning (864) and Manning (503) are directed to different types of memory (i.e., asynchronous vs. synchronous), and combining them defeats the purpose of the devices disclosed in each case.

Several statements of alleged fact, unsupported by any reference, are presented in the Answer. While the Appellants have repeatedly requested evidentiary support for similar statements, none has been given. A few of these statements are quoted below:

- (a) "it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input, or memory data output to be processed simultaneously";
- (b) "the pipelined architecture requires only a single sample-and-hold circuit per read or write circuit"; and
- (c) "pipelined architecture can be used on standard EDO, fast page mode, static column, and burst modes (see col. 7 lines 50-54)".

However, other than these unsupported statements, there is no evidence whatsoever that Manning (864) or Manning (503) teach this specific type of operation or construction. The text of Col. 7, lines 50-54 merely states "A more complex memory device may provide additional modes ... such as switching between fast page mode, EDO page mode, static column mode and burst operation through the use of various combinations of /WE and /OE at /RAS falling time." This is obviously not a reference to a pipelined mode of operation. Further, as explained in the Appeal Brief (see Appeal Brief pgs. 11-12), and in the reference cited by the Appeal Brief (see Appeal Brief, Appendix II), none of these modes necessarily have anything to do with a true pipelined mode of operation. Thus, the assertion that either Manning (864) or Manning (503) teaches a pipelined mode of operation is simply not supported by the evidence in the record.

The Appellants are unable to address the argument which is included in the second full paragraph of pg. 9 of the Answer. The following statement is made: "Synchronous operation

mention [sic] in the 503 reference is synchronous burst address generation in response to the CAS transition although an initial external address is inputted in [sic] asynchronously." The Appellants are unsure of what this statement is supposed to indicate. However, it is very clear from the title of Manning (503) that synchronous devices are addressed by that patent, and this is not contradicted by this statement.

Finally, it is respectfully noted that a Notice of Allowability (the "Notice") indicating allowance of all claims was mailed to the Appellants (Paper 32) in U.S. Patent Application Serial Number 08/984,561; Atty. Ref:303.623US6, the appeal of which is no longer before the Board. The Office has admitted the deficiencies of Manning (864) in this related matter with respect to several elements claimed by the Appellants in the instant Application. The attention of the Board is directed to the following assertions by the Appellants in the appeal of U.S. Application Serial No. 08/984,561:

"Manning Col. 6, lines 14-34 merely describe burst and "standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Manning Col. 7, lines 43-54 speaks to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Thus, **Manning never discusses the ability to select or switch between burst and pipelined modes of operation...**" (emphasis added)

This language was approved by the Office in the Notice, which states: "The claims are allowable over the prior art of record [U.S. Patent No. 5,587,964, issued to Rosich et al. in view of Manning (864)] because the claims are distinguished from the prior art of record for the reasons as set forth in the ... appeal filed on 12/27/02 and because an update of a search previously made does not detect the combined claimed elements as set forth in claims 1-23." For example, claim 72 of U.S. Application Serial No: 08/984,561 reads:

A method for switching between pipeline and burst modes of operation, comprising:
maintaining a first enabling signal in an active state, the first enabling signal being an address-strobe signal;
maintaining an external mode select signal to select a pipeline mode;
receiving a stream of addresses and cycling a second enabling signal for processing the stream of addresses; and

switching the mode of operation to a burst mode on successive cycles of the second enabling signal while maintaining the first enabling signal in the active state.

Thus, the Office agrees that Manning (864) does not teach the ability to select or switch between burst and pipelined modes of operation.

Response by the Appellants to Specific Arguments in the Answer

Specific references to claims in the Answer are separated into ten groups. To simplify coordinating the responses to these arguments, the Appellants will reply in accordance with the grouping. However, this response format is in no way to be construed as an admission that such grouping is appropriate, as alleged in the Answer. The response for each group will be presented in the form of a statement in the Answer, and a factual correction in the response.

Group I:

Statement -- Manning discloses ... circuitry for switching or selecting between a burst mode and a pipelined mode ... switching between burst EDO mode and standard EDO mode read on this limitation.

Response -- As noted in the reference cited by the Appeal Brief, including the burst mode in a memory may result in the addition of a pipeline stage to permit reads/writes to occur in four row address bursts. However, burst EDO memory including a pipelined architecture/stage does not "accept external addresses so as to operate in a pipelined mode" as defined by the Appellants in the Application.

Group II:

Statement -- Manning (864) discloses an external mode select signal (col. 6 lines 14+ and col. 7 lines 44-54 and Fig. 1).

Response -- As noted above, the Office has already admitted that "Manning [864] does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." with respect to Application Ser. No. 08/984,701, Paper

19, page 7. Further, as noted above, the Office has agreed with the Appellants in the appeal of U.S. Application Serial No: 08/984,561 that Manning (864) does not disclose any way to switch between pipelined and burst modes.

Group III:

Statement – Manning (864) discloses using write enable and a separate output enable signal for determining the mode control signal.

Response – Manning teaches using a write enable and output enable signals to switch modes, but not “... for receiving ... the selected mode control signal ... therefrom and for switching the memory circuit between a burst mode and *a pipelined mode*” as claimed by the Appellants.

Group IV:

Statement – Manning (864) discloses using a second external address subsequent to a first external address. ... Manning reads on this limitation since the second address should be provided subsequent to the first address in a pipelined mode of operation.

Response – The assertion in this case is unsupported by any evidence in the record. Nothing in Manning (864) describes this specific method of operation, as admitted in the Answer (which resorts to the use of the word “should” when describing this type of operation, rather than a specific reference to the text of Manning).

Group V:

Statement – Manning (864) discloses the pipelined mode as being an EDO mode.

Response – As admitted in the second paragraph of the Answer, pg. 13, “Manning (864) discloses ... switching between burst EDO mode and standard EDO mode”. Asserting that the pipelined mode is necessarily the same as an EDO mode clearly contradicts the reference supplied by the Appellants in Appendix II of the Appeal Brief, and is not supported by the text of Manning (864), nor by the text of the Answer itself.

Group VI:

Statement – Manning (864) discloses any type of address strobe latency in conjunction with a pipelined mode of operation ... col. 5 lines 43-49.

Response – The teaching of Manning in the referenced text might be directed to a burst EDO memory pipeline stage. However, there is nothing in the reference or in this record to indicate the cited text of Manning (864) refers to a pipelined mode of operation as defined by the Appellants.

Group VII:

Statement – ... during the burst mode, an internal counter/latch path is selected however, during pipelined mode, an external counter/latch path is selected.

Response – There is no evidence in the record that Manning (864) teaches a pipelined mode of operation in conjunction with selecting an external counter/latch path.

Group VIII:

Statement – Manning discloses a counter (Fig. 1, Ref. 26).

Response – The mere existence of a counter in Manning (864), without more, is insufficient to satisfy the requirements of § 102, since “The *identical invention* must be shown in as complete detail as is contained in the ... claim.” *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131. There is no evidence in the record that the counter of Manning (864) is for “switching the memory circuit between a burst mode and a pipelined mode” as claimed by the Appellants.

Group IX:

Statement – Manning (864) discloses asynchronously accessible random access memory.

Response – The mere use of the term “asynchronous” in conjunction with memory in Manning (864), without more, is insufficient to satisfy the requirements of § 102, since “The *identical invention* must be shown in as complete detail as is contained in the ... claim.” *Id.* There is no evidence in the record that the memory described by Manning (864) is able to switch “between a burst mode and a pipelined mode” as claimed by the Appellants. Again, noted

above, the Office has agreed with the Appellants in the appeal of U.S. Application Serial No: 08/984,561 that Manning (864) does not disclose any way to switch between pipelined and burst modes.

Group X:

Statement – Manning (503) discloses a first external address (Fig. 5 Ref. 305), a first multiplexer (Fig. 5 Ref. 350), a second external address (Fig. 5 Ref. 320) and a second multiplexer (Fig. 5 Ref. 370).

Response – The mere use of the terms “address” in conjunction with one or more multiplexers in Manning (503), without more, is insufficient to satisfy the requirements of § 102, since “The *identical invention* must be shown in as complete detail as is contained in the ... claim.” *Id.* There is no evidence in the record that the addresses described by Manning (503) are available so that “each multiplexer selects its respective external address when the selected mode control signal indicates a pipeline mode, and each multiplexer selects a supplied internal address when the selected mode control signal indicates a pipelined mode” as claimed by the Appellants. In fact, it is clear that neither multiplexer of Manning (503) operates to “receive a selected mode control signal” as claimed by the Appellants. For example, the multiplexer 370 shown in FIG. 5 receives only address signals. Again, noted above, the Office has agreed with the Appellants in the appeal of U.S. Application Serial No: 08/984,561 that Manning (864) does not disclose any way to switch between pipelined and burst modes. Neither does Manning (503).

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Title: MEMORY DEVICE FOR BURST OR PIPELINED OPERATION WITH MODE SELECTION CIRCUITRY

CONCLUSION

For these reasons, it is respectfully submitted that neither has a *prima facie* case of anticipation under 35 U.S.C. §102 been established, nor has a *prima facie* case of obviousness under 35 U.S.C. §103 been established. Therefore, it is respectfully requested that the rejection of claims 22-32, 59, 61, 63, and 66-72 be reconsidered and withdrawn so that the claims will be in condition for allowance.

The Examiner is invited to telephone Appellants' attorney, Mark Muller, at (210) 308-5677, or the undersigned to facilitate prosecution of this Application. Should the Board be of the opinion that any rejected claim is allowable in amended form, an explicit statement to that effect is also respectfully requested. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JEFFREY S. MAILLOUX ET AL.

By their Representatives,

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By 

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Applicant: Jeffrey S. Mailloux et al.

Title: MEMORY DEVICE FOR BURST OR PIPELINED OPERATION WITH MODE SELECTION CIRCUITRY

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Group Art Unit: 2186

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